When to worry about trace corners: Rule of Thumb #24

Eric Bogatin - February 04, 2015

Spoiler summary: A corner will affect the signal when the line width in mils > 5× the rise time in picoseconds.

Remember: before you start using rules of thumb, be sure to read the Rule of Thumb #0: Use rules of thumb wisely.

Previous: When to worry about a capacitive discontinuity: Rule of Thumb #23

The poster child for why you have to worry about the signal integrity in interconnects is “corners cause reflections and they should be avoided in high speed designs.”

In many of my introductory classes and even my graduate class, I encounter this recommendation from students and engineers who have never taken a signal integrity class, but have picked up what they know from the street.

There are a lot of columns written on this topic, but in some of them, I am at a loss to understand what their reasoning is, or they look at a specific special case, providing no insights to apply to any other situation.

Let me try to set the record straight. Do corners affect signals? Absolutely. But are they a problem? It depends.

In this rule of thumb, we’re going to look at answering the question: When do corners affect signals? Hint: it has nothing to do with electrons accelerating around the bend. Its root cause is much more mundane.

Of course, some fab houses recommend to not use 90° corners on traces but to make all bends 45°, not for signal integrity reasons, but for reliability. They will say that the inside bend of a 90 degree corner will collect some hard-to-clean-out acid used in etching the lines, which will be a source of contamination which will corrode the trace when left on the shelf in a humid environment. If your fab vendor tells you this, find another fab vendor.

To understand the electrical impact from a corner, consider a rounded bend which keeps a constant line width as the signal turns the corner. Since the line width is fixed, there is no impedance change and the signal has no idea it is turning a corner.

Now, make the bend 90 degrees. The line width is no longer constant. It is wider at the bend, which means, since the dielectric thickness is fixed, the impedance will be lower. The bend acts as an

extra, small, discrete capacitor on the otherwise uniform line width. We can estimate this excess capacitance. Figure 1 illustrates how.

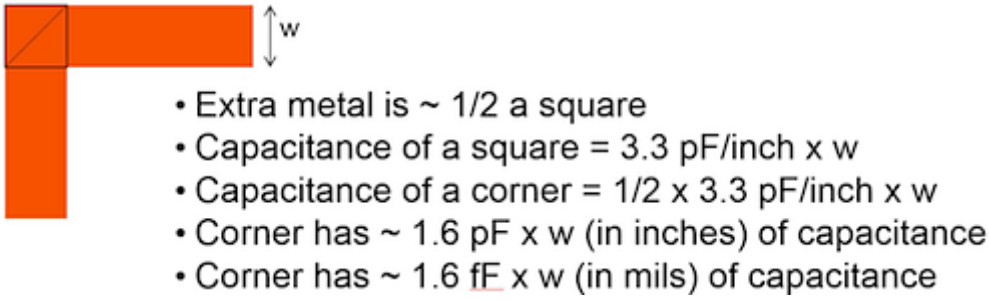

Figure 1 Estimating excess corner capacitance

Let's make the simplifying assumption that a corner has half a square of extra metal above and beyond what would be there if we had a uniform line width bend. How much capacitance is this?

Like most questions in signal integrity, the answer is, "it depends." That's why it's so important to be able to make quick, simple estimates.

In a 50Ω transmission line, the capacitance per length is about 3.3pF/in. This is independent of the line width or any other feature, other than it is a 50Ω line and made with FR4 (see RoT #5).

The length of a square is just the line width, w. If the line is wider, to keep the 50Ω impedance, the dielectric thickness also has to increase. The capacitance per length stays the same, but the length of the square is longer, so the capacitance in a square increases. The excess capacitance is half a square, so the capacitance is 1.6fF × w, with w in mils .This is about 2fF/mil × w.

This is the origin of the rule of thumb:

> *The excess capacitance in a corner is 2fF/mil × w[mils].*

As a quick test of this simple model, I built a 50Ω line in a 2 layer board, with 4 corners. The board was 32mils thick and the line width was 60mils. The excess capacitance in each corner was about 120fF. This can easily be measured with a TDR. The capacitance causes a dip in the reflected signal. From the dip, I can extract the excess capacitance. Figure 2 shows the result.

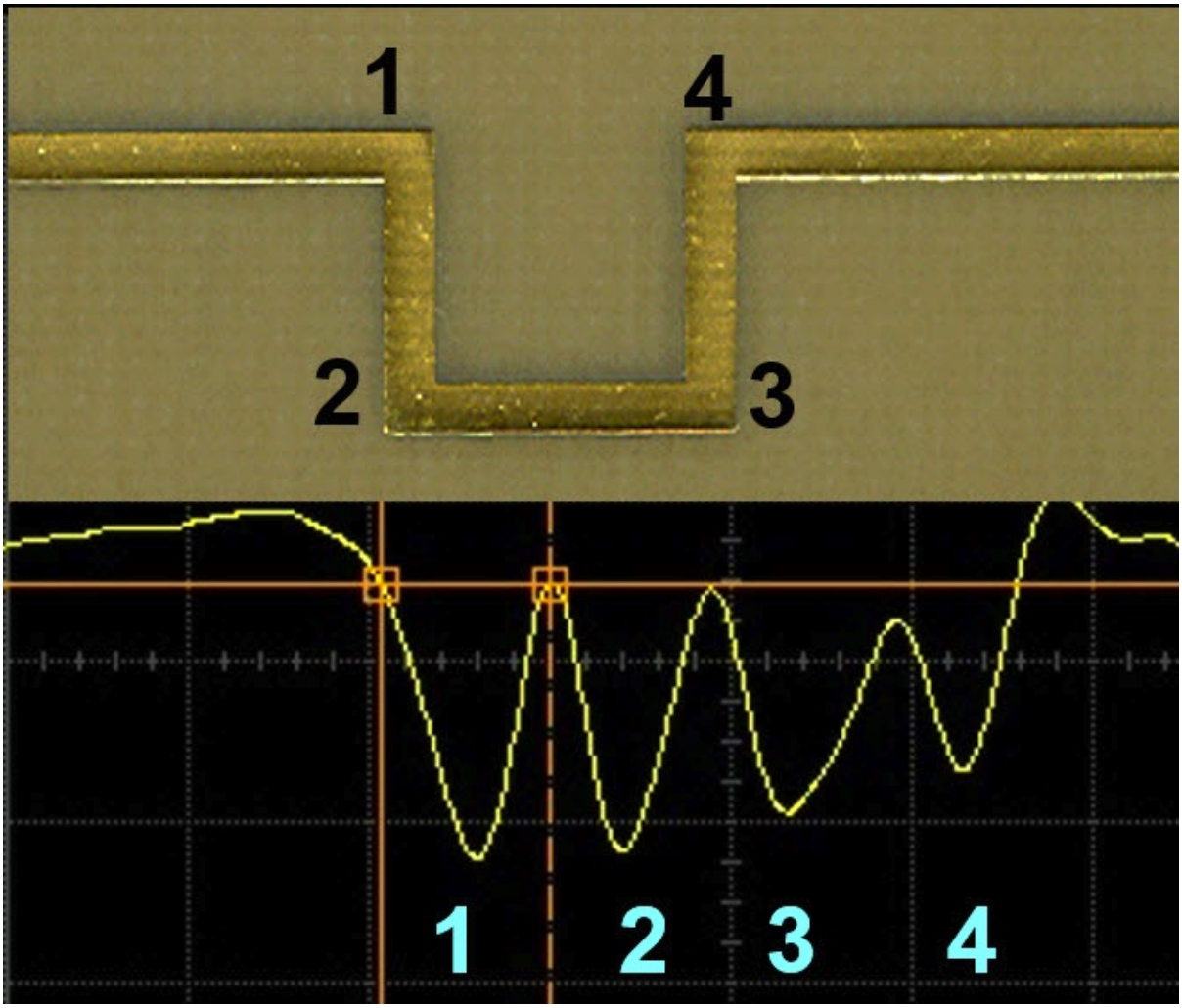

Figure 2 Test PCB and TDR response

Each dip in the TDR trace is the reflection from each corner. Clearly a corner causes reflections. But the scale is dramatically increased in this TDR trace. The rise time is 40ps and the scale is 5% per division. From this measurement, I can extract the excess capacitance – it is 96fF. This is very close to our estimate of 120fF for the 60mil wide trace. Not a bad rule of thumb.

Now that we can estimate the excess discrete capacitance in a corner, we can answer the question: When do we have to worry? Rule of Thumb #23 said: If the capacitance, in femtofarads, is greater than 10× the signal rise time in picoseconds, worry about the capacitance. This translates to worry about the impact from corners when:

$$2\text{fF/mil} \times w[\text{mils}] > 10 \times RT[\text{ps}], \text{ or, } w[\text{mils}] > 5 \times RT[\text{ps}]$$

If your rise time is 10ps, don't worry about corners unless your 50Ω line widths are wider than 50mils.

Now you try it:

1. If the rise time is 100ps, at what line width should you worry about corners?
2. If the line width is 5mils, at what rise time should you worry about corners?

Also see:

- Bogatin's Rules of Thumb
- Who's afraid of the big, bad bend?

Additional information on this and other signal integrity topics can be found at the Signal Integrity Academy, www.beTheSignal.com.